# IMAGING ARRAY UTILIZING THYRISTOR-BASED PIXEL ELEMENTS

This is a continuation-in-part of U.S. Serial No. 09/556,285 to Taylor, filed April 24, 2000 and entitled "A III-V Charge Coupled Device Suitable for Visible Near and Far Infrared Detection", and a continuation-in-part of International Application No. PCT/US02/06802 to Taylor filed March 4, 2002, and a continuation-in-part of International Application No. PCT/US03/13183 to Taylor filed April 28, 2003, all of which are hereby incorporated by reference herein in their entireties.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to optoelectronic devices. More particularly, the present invention relates to imaging arrays based on charged coupled devices (CCD) formed from semiconductors such as gallium arsenide (GaAs) which are capable of generating electrical signals in response to light. The invention is particularly applicable to the imaging and the telecommunications arts, although it is not limited thereto.

### 2. State of the Art

In the imaging arts, next generation imaging systems must operate at very high frequencies and have a high resistance to radiation flux such that the imager is said to be "radiation hardened." State-of-the-art imagers are constructed as silicon integrated circuits in the form of CCDs or active pixel arrays. In the CCD, a linear array of pixels is clocked sequentially to a common output amplifier. In the active pixel array, the array is x-y addressable and each pixel is output to its own dedicated amplifier (the array is output on a row by row or column by column basis).

Silicon technology is limited by the presence of the silicon oxide in both the active and passive regions of the integrated circuit in a number of ways. A main limitation is the sensitivity of the oxide to radiation flux. The radiation creates traps and other charged defects in the insulator which alter the internal voltage thresholds in both active and passive regions within the

1   integrated circuit. After a certain cumulative exposure level, these threshold changes render the

2   circuit inoperable. The gate oxide creates limitations in other ways as well. The silicon CCD

3   couples one pixel to the other via overlapping gates. Each overlapping gate creates a small region

4   of thicker oxide between pixels which inhibits charge transfer and therefore sets a speed

5   limitation upon the CCD. These oxide barriers are fundamental to the silicon CCD and

6   constitute a transfer speed limitation. Some approaches have been employed to eliminate these

7   effects such as the virtual phase CCD. However, these structures are then faced with barriers

8   created by implant misalignment and a lack of well capacity. In any event the transfer speed in

9   the silicon CCD rarely exceeds a few MHz.

10

11      A further limitation of the silicon CCD is its spectral sensitivity. The silicon CCD

12  absorbs radiation across its energy gap and therefore is insensitive to radiation with a wavelength

13  longer than about 1um. It is also insensitive to ultraviolet (UV) radiation.

14

15      As disclosed in parent application U.S. Serial No. 09/556,285, III-V device structures

16  based upon GaAs substrates have the potential to overcome the above limitations. In particular,

17  the GaAs CCD has the potential to absorb electromagnetic energy within a quantum well

18  between the various subbands. This provides the GaAs device with unique capabilities of

19  intersubband absorption and sensitivity in the mid wavelength infrared, long wavelength infrared

20  and very long wavelength infrared regions. The GaAs device structures that currently perform

21  the intersubband detector functions are the QWIP (quantum well infrared photodetector) devices.

22  Two significant limitations of the QWIP as currently implemented are the existence of a

23  significant level of dark current that necessitates cooling of the device to 77°K, and the fact that

24  the device is not compatible with GaAs integrated circuits. When originally demonstrated, the

25  QWIP was considered advantageous because of its potential compatibility with GaAs integrated

26  circuits. However, this compatibility has never been established and so present technology

27  combines the GaAs QWIP wafer in a hybrid fashion with a Si read-out integrated circuit.

28

29      There have been several efforts to build CCD shift registers using the basic transistor

30  structures of the MESFET (metal semiconductor field effect transistor) and HEMT (high electron

31  mobility transistor) devices. See Song et al., "A Resistive-Gate $Al_{0.3}Ga_{0.7}As$/GaAs 2DEG CCD

1   with High Charge-Transfer Efficient at 1 GHz," IEEE Transactions on Electron Devices, Vol.

2   38, No. 4, April 1991, pgs. 930-932; Ula et. al., "Simulation, Design and Fabrication of Thin-

3   Film Resistive-Gate GaAs Charge Coupled Devices," Electron Devices Meeting, 1990, pgs. 271-

4   274; Bakker et al., "A Tacking CCD: a New CCD Concept," IEEE Transactions on Electron

5   Devices, Vol. 38, No. 5, May 1991, pgs. 1193-1200; Davidson et al., "GaAs charge-coupled

6   devices", Can. J. Physics, Vol. 67, 1989, pgs. 225-231; Song et al., "Characterization of

7   Evaporated Cr-SiO cermet films resistive-gate CCD applications," IEEE Transactions on

8   Electron Devices, Vol. 36, No. 9, Sept. 1989, pgs. 1575-1597; LeNoble et al., "A Two-Phase

9   GaAs Cermet Gate Charge-Coupled Device," IEEE Transactions on Electron Devices, Vol. 37,

10  No. 8, Aug. 1990, pgs. 1796-1799; Beggs et al., "Optical charge injection into a gallium arsenide

11  acoustic charge transport device," Journal of Applied Physics, Volume 63, Issue 7, 1988, pgs.

12  2425-2430; Ablassmeier et al., "Three-phase GaAs Schottky-barrier CCD Operated up to 100-

13  MHz Clock Frequency," IEEE Transactions on Electron Devices, Vol. 27, No. 6, June 1980, pgs.

14  1181-1183; LeNobel et al., "Uniphase operation of a GaAs resistive gate charge-coupled

15  device," Can. J. Physics, Vol. 70, 1992, pgs. 1143-1147; LeNobel et al., "Two-Phase GaAs

16  cermet-gate charge-coupled devices," Can. J. Physics, Vol. 69, 1991, pgs. 224-227; Ula et al.,

17  "Optimization of thin-film resistive-gate and capacitive-gate GAAs charge-coupled devices,"

18  IEEE Transactions on Electron Devices, Vol. 39, No. 5, May 1992, pgs. 1032-1040; and

19  LeNoble et al. "The Surface Potential Variation in the Interelectrode Gaps of GaAs Cermet-gate

20  Charge-Coupled Devices," Solid-State Electronics, Vol. 33, No. 7, 1990, pgs. 851-857. These

21  technologies have always been plagued by the problem of low transfer efficiencies between

22  pixels in the array. The proposed solutions utilize a resistive coupling between pixels, which

23  would provide drift aided transfer. The problem has been that no viable technique to implement

24  resistive coupling has been found. The use of deposited resistive layers was attempted but the

25  resistive control problems discouraged further investigations.

26

27      Parent application U.S. Serial No. 09/556,285 overcomes many of these problems by

28  providing a CCD having an epitaxial growth structure which utilizes a modulation doped

29  quantum well interface to create an inversion channel for the storage of charge packets. The

30  charge transfer is facilitated by the unique features of the epitaxial growth which include two

31  delta-doped sheets of p-type doping. One p type sheet is very close to the inversion channel and

1   enables a resistive coupling between adjacent pixels through a very thin sheet of highly doped

2   material. The resistive coupling enables a high field and optimized drift velocity between pixels

3   during the transfer phase which is responsible for the very high transfer rate. The second charge

4   sheet positioned at the wafer surface enables a very low resistance ohmic contact to the top

5   metal contact. It is this ohmic contact that enables the HFET, which is the fundamental field

6   effect device in the technology. The inversion channel is comprised of multiple quantum wells

7   and these quantum wells may absorb incident radiation in the MWIR (mid-wave infrared) and

8   LWIR (long-wave infrared) regions. The CCD may also image signals in the UV, the visible and

9   the near IR regions of the spectrum by conventional band gap absorption.

10

11         In the CCD device of the parent application Serial No. 09/556,285, a refractory emitter

12   or gate metal contact is used for the transfer portion of the pixel. Also, dielectrics are used above

13   the gate to form 1/4 wavelength pairs for the imaging portion of the pixel. These dielectrics,

14   when taken together with an epitaxially grown mirror below the active device structure constitute

15   a resonant cavity at the wavelength of interest. In the described embodiments, ion implants are

16   used for several purposes. An N type implant is used to form source and drain regions to the

17   inversion channel, and it is also used to shift the threshold voltage of the inversion channel

18   interface. The epitaxial structure is grown as a normally off (enhancement) device and then the

19   N type implant is used to create regions of normally on (depletion) devices and it is these regions

20   where the charge packets are stored. Oxygen implants may also be used to create high resistance

21   regions below the implants. The technology utilizes the oxidation of AlAs and other layers with

22   large aluminum percentages to achieve passivation, isolation and dielectric mirrors below the

23   structure. The basic structure of the pixel and the output amplifiers which are employed in the

24   CCD may also be used to design an active pixel sensor. In such a design, each pixel is interfaced

25   to an output amplifier and a row or a column is output in parallel.

26

27         While the devices disclosed in parent application U.S. Serial No. 09/556,285 represent

28   major advances over the prior art and provide practical solutions to the problems of the prior art,

29   the disclosed devices still suffer from certain limitations. For example, with the provided

30   structure, it can take one millisecond or so for electrons to remove themselves from the quantum

31   wells in response to received light, and so the speed of the imaging process is limited by that

1   timing. In addition, because the read-out signal generated by the disclosed device for a given

2   period is the amount of charge remaining in the quantum wells, the read-out signal is large when

3   the well is relatively full; i.e., when the light was weak. Thus, a weak signal is possibly

4   undesirably subjected to a relatively large amount of noise.

5

6   <div align="center">SUMMARY OF THE INVENTION</div>

7

8   It is therefore an object of this invention to provide an imaging array of pixel element,

9   preferably utilizing a III-V semiconductor system, which is capable of very high transfer rates.

10

11   It is another object of the invention to provide an imaging array of pixel elements which

12   can be adapted to absorb electromagnetic radiation in the broad spectral range from 3um–20um

13   via intersubband absorption and convert the radiation to packets of charge for output therefrom.

14

15   It is a further object of this invention to provide an imaging array of pixel elements which

16   can be adapted to absorb electromagnetic radiation in the ultra-violet, visible and near infra-red

17   portions of the electromagnetic spectrum via bandgap absorption and convert the radiation to

18   packets of charge for output therefrom.

19

20   It is an additional object of this invention to implement the imaging array of pixel

21   elements in an integrated fashion together with HFET technology.

22

23   Another object of this invention to implement the imaging array of pixel elements as part

24   of a monolithic optoelectronic integrated circuit that includes additional optoelectronic circuitry

25   and/or electronic circuitry.

26

27   In accord with the objects of the invention, an imaging array (and corresponding method

28   of operation) is provided having an epitaxial growth structure with complementary types of

29   modulation doped quantum well interfaces; one which creates an inversion channel for electrons,

30   and one which creates an inversion channel for holes. The epitaxial growth structure is

31   preferably the same structure disclosed in previously incorporated U.S. Serial No. 09/798,316

1    which relates to a modulation doped thyristor. More particularly, two modulation doped

2    quantum well structures which are separated from each other are located below a p+ layer and

3    above an n+ layer. The first modulation doped quantum well structure (referred to as the "n-type

4    modulation doped quantum well interface) creates an inversion channel for the electrons, while

5    the second modulation doped quantum well structure (referred to as the "p-type modulation

6    doped quantum well interface) creates an inversion channel for holes. Dielectrics are used above

7    the top p+ layer and below the bottom n+ layer to form 1/4 wavelength pairs for the imaging

8    portion of the pixel; i.e., they constitute a resonant cavity at the wavelength of interest.

9

10    In a preferred embodiment, the pixel elements of the imaging array are metallized as

11    follows. For each pixel element, a refractory anode terminal is formed adjacent the highly doped

12    top p+ layer; i.e., the top "p" structure. The anode terminal is used to control the transfer of

13    charge into and/or from the pixel element. A p-channel injector terminal is operably coupled to

14    the p-type modulation doped quantum well interface, and a cathode terminal is operably coupled

15    to the bottom n+ layer. The p-channel injector terminal is used to empty the p-type quantum

16    well interface of charge (e.g., holes). The cathode terminal is used to realize an electronic shutter

17    that enables/disables the charge accumulation operations of the pixel element.

18

19    The pixel elements operate in three distinct modes: pixel setup mode; signal acquisition

20    mode; and signal transfer mode. During pixel setup mode, the n-type quantum well interface is

21    emptied of charge (e.g., electrons). During signal acquisition mode, charge is accumulated in the

22    n-type quantum well interface of the pixel element. The amount of accumulated charge is

23    proportional to the amount of electromagnetic radiation at the desired wavelength that is received

24    at the pixel element. During signal transfer mode, the accumulated charge is read out from the

25    pixel element (and transferred between pixel elements in CCD-type applications) utilizing the n-

26    type quantum well interface as the pathway for charge transfer. In CCD-type applications, an n-

27    channel injector contact that contacts the n-type quantum well interface for the last pixel element

28    is the output of the imaging array and may be amplified directly if desired.

29

30    Further features and advantages of the invention will become more readily apparent from

31    the following detailed description when taken in conjunction with the accompanying drawings.

1

2 BRIEF DESCRIPTION OF THE DRAWINGS

3

4 FIG. 1 is a schematic view showing an exemplary quantum-well base bipolar transistor

5 device.

6

7 FIG. 2 is an energy band diagram illustrating the operation of the quantum-well base

8 bipolar transistor device of FIG. 1 in response to radiation supplied to the quantum well base

9 region of the device.

10

11 FIG. 3A is a schematic view showing two exemplary thyristor-based pixel elements in

12 accordance with the present invention.

13

14 FIG. 3B is an energy band diagram illustrating the operation of the thyristor-based pixel

15 element of FIG. 3A in response to incident radiation that is resonantly absorbed therein.

16

17 FIGS. 4A, 4B and 4C are energy band diagrams illustrating the operational modes of the

18 thyristor-based pixel elements of FIG. 3A during an imaging cycle whereby charge is

19 accumulated in and transferred out of a respective pixel element in accordance with the present

20 invention.

21

22 FIG. 5 illustrates an exemplary epitaxial growth structure utilizing group III-V materials

23 for realizing the thyristor-based pixel element of FIG. 3A and the optoelectrical/electrical/optical

24 devices formed from this structure in accordance with the present invention.

25

26 FIGS. 6A, 6B1 and 6B2 are schematic views of an exemplary realization of two thyristor-

27 based pixel elements formed in conjunction with the epitaxial growth structure of FIG. 5; FIG.

28 6A is a schematic plan view of the two thyristor-based pixel elements; FIG. 6B1 is a schematic

29 cross-sectional view of the two thyristor-based pixel elements; and FIG. 6B2 is a schematic

30 cross-sectional view of the p-channel injector terminal for the two thyristor-based pixel elements.

31

1    FIG. 6C is a diagram illustrating the potential along the n-type modulation doped

2    quantum well interface within (and between) the two thyristor-based pixel elements of FIGS. 6A

3    and 6B during the imaging operations performed by these pixel elements.

4

5    FIG. 7A is a functional block diagram illustrating the system architecture of a full-frame-

6    type imaging array.

7

8    FIG. 7B is a functional block diagram illustrating the system architecture of an interline-

9    type imaging array.

10

11    FIG. 8A is a schematic cross-sectional view of an exemplary realization of a thyristor-

12    based pixel element and transfer gate formed in conjunction with the epitaxial growth structure

13    of FIG. 5.

14

15    FIG. 8B is a diagram illustrating the potential along the n-type modulation doped

16    quantum well interface within (and between) the thyristor-based pixel element and transfer gate

17    of FIG. 8A during the imaging operations performed by the pixel element.

18

19    FIG. 8C is a functional block diagram illustrating the system architecture of an active-

20    pixel-type imaging array utilizing pixels based on the thyristor-based pixel element and transfer

21    gate of FIGS. 8A and 8B.

22

23    DESCRIPTION OF THE PREFERRED EMBODIMENTS

24

25    In accordance with the present invention, an imaging device is provided that includes

26    complementary modulation doped quantum well interfaces formed between a top p+ layer

27    structure and bottom n+ layer structure. Dielectrics are used above the top p+ layer and below

28    the bottom n+ layer to form 1/4 wavelength pairs for the imaging portion of the pixel; i.e., they

29    constitute a resonant cavity at the wavelength of interest. In the preferred embodiment, each

30    pixel element is formed from a mesa that includes a refractory anode terminal formed adjacent

31    the highly doped top p+ layer structure. The anode terminal is used to control the transfer of

1    charge into and/or from the pixel element. A p-channel injector terminal is operably coupled to

2    the p-type modulation doped quantum well interface, and a cathode terminal is operably coupled

3    to the bottom n+ layer. The p-channel injector terminal is used to empty the p-type quantum

4    well interface of charge (e.g., holes). The cathode terminal is used to realize an electronic shutter

5    that enables/disables the charge accumulation operations of the pixel element.

6

7    The pixel elements operate in three distinct modes: pixel setup mode; signal acquisition

8    mode; and signal transfer mode. During pixel setup mode, the n-type quantum well interface is

9    emptied of charge (e.g., electrons). During signal acquisition mode, charge is accumulated in the

10    n-channel quantum well interface of the pixel element. The amount of accumulated charge is

11    proportional to the power of the electromagnetic radiation at the desired wavelength that is

12    received at the pixel element during the signal acquisition mode. During signal transfer mode,

13    the accumulated charge is read out of the given pixel element (and transferred between pixel

14    elements in CCD-type applications) utilizing the n-type quantum well interface as the pathway

15    for charge transfer. In CCD-type applications, an n-channel injector contact that contacts the n-

16    type quantum well interface for the last pixel is the output of the imaging array and may be

17    amplified directly if desired.

18

19    The imaging array of the present invention (and the signals produced therefrom) can be

20    used in many applications. For example, it can be used to perform imaging operations over

21    nanosecond to millisecond time increments (due to the high speed of response of the 2D gas).

22    Moreover, it can readily be adapted to image wavelengths over a broad spectrum of wavelengths

23    (including mid-infrared wavelengths as well as long-infrared wavelengths). Moreover, the

24    imaging array of the present invention can be efficiently integrated with a broad range of optical

25    and electronic devices, for example to provide an integrated array together with associated

26    optoelectronics and/or logic circuits and/or signal processing circuits.

27

28    Preferably, the imaging array of the present invention (and possibly other optoelectronic

29    devices, logic circuits and/or signal processing circuits that are fabricated integral thereto) are

30    realized from the inversion quantum-well channel device structures as described in detail in U.S.

31    Patent 6,031,243; U.S. Patent Application No. 09/556,285, filed on April 24, 2000; U.S. Patent

1   Application No. 09/798,316, filed on March 2, 2001; International Application No.

2   PCT/US02/06802 filed on March 4, 2002; U.S. Patent Application No. 08/949,504, filed on

3   October 14, 1997, U.S. Patent Application No. 10/200,967, filed on July 23,2002; U.S.

4   Application No. 09/710,217, filed on November 10,2000; U.S. Patent Application No.

5   60/376,238, filed on April 26, 2002; U.S. Patent Application No. 10/323,390, filed on December

6   19, 2002; U.S. Patent Application No. 10/280,892, filed on October 25, 2002; U.S. Patent

7   Application No. 10/323,390, filed on December 19, 2002; U.S. Patent Application No.

8   10/323,513, filed on December 19, 2002; U.S. Patent Application No. 10/323,389, filed on

9   December 19, 2002; U.S. Patent Application No. 10/323,388, filed on December 19, 2002; U.S.

10  Patent Application No. 10/340,942, filed on January 13, 2003; all of which are hereby

11  incorporated by reference in their entireties. With these structures, a fabrication sequence is used

12  to make all the devices, including the imaging array, electrical devices (e.g., transistors) and

13  optoelectronic devices (e.g., laser/detector/modulator) on a common substrate. In other words, n

14  type and p type contacts, critical etches, dielectric depositions etc. are used to realize all of these

15  devices simultaneously on a common substrate. The essential features of this device structure

16  include 1) an n-type modulation doped interface and a p-type modulation doped quantum well

17  interface, 2) self-aligned n-type and p-type channel contacts formed by ion implantation, 3) n-

18  type metal contacts to the n-type ion implants and the bottom n-type layer structure, and 4) p-

19  type metal contacts to the p-type ion implants and the top p-type layer structure.

20

21      The state of the charge in the n-type modulation doped quantum well interface and p-type

22  modulation doped quantum well interface is controlled by conduction from either the anode or

23  cathode as dictated by the bias conditions of the thyristor device. In addition, charge may be

24  removed from the n-type modulation doped quantum well interface and p-type modulation doped

25  quantum well interface by a current source (or pulse source) electrically coupled to the injector

26  terminal for the respective interface. Optical devices are created from these structures by

27  separating the metal anode into two sections which are connected electrically by the P+ layer

28  along the top surface. The active device structure is formed between a bottom distributed bragg

29  reflective (DBR) mirror and a top dielectric mirror, thereby forming a waveguide with an optical

30  mode centered near the modulation doped quantum well interfaces.

31

1    A cross-section of a quantum-well-base bipolar transistor is shown in FIG. 1. The

2    quantum-well-base bipolar transistor is interesting because of the way in which it combines the

3    unipolar conduction of a typical Heterojunction FET (HFET) device and the bipolar conduction

4    of a typical Heterojunction Bipolar Transistor (HBT). It is, in fact, a quantum-well-base bipolar

5    transistor based upon modulation doping. The contacts to the modulation doped channel perform

6    as source/drain contacts of a typical HFET with gate bias applied in the conventional way. The

7    channel charge performs as the minority charge of a bipolar transistor. Then, as the charge flows

8    into the channel it biases the internal barrier of the device to the flow of majority carriers from

9    the emitter into the collector. Because of its combination of bipolar and FET principles, the

10   device is sometimes referred to as a Bipolar Inversion Channel Field Effect Transistor

11   (BICFET). Advantageously, the thermionic emission in the quantum-well-base bipolar transistor

12   occurs vertically in the epitaxial growth direction and the distances are short (on the order of 100

13   Å) so that cutoff frequencies above 1 THz can be obtained without the need for extremely short

14   lithographic dimensions of the device.

15

16   The device includes, starting from a semi-insulating substrate 10, an n+ GaAs contact

17   layer 12 (which is electrically connected to a subcollector terminal metal layer 13), an n-type

18   AlGaAs layer 14, a p-type AlGaAs layer 16 (which is electrically connected to a collector

19   terminal metal layer 17), an n-type modulation doped quantum well structure 18 (which is

20   electrically connected to base terminal metal layer 19 via n-type ion implants 21), an undoped

21   spacer layer 20, a p+-type charge sheet 22, a p-type barrier layer of AlGaAs 24, and a P+ contact

22   layer 26 of GaAs (which is electrically connected to emitter terminal metal layer 27). Received

23   radiation is operably coupled to the n-type modulation doped quantum well structure 18 via the

24   base terminal metal layer 19.

25

26   The responsivity of the device of FIG. 1 depends upon the change of the electron

27   temperature of the 2D gas ($T_e$) with input power $P_{in}$ of the received radiation. This relationship

28   can be understood by the following analysis. If an electron (or hole) is represented by its

29   equation of motion in the presence of a perturbing electric field $E_0 e^{jwt}$, and one solves for

30   displacements of the electron $x_0 e^{jwt}$, then one can solve for the velocity, the current flow and the

31   average power absorbed by the RF field. In the steady state, this is balanced by the heat lost to

1    the lattice by the emission of polar optical phonons. From this energy balance we obtain the

2    result

3
$$\Delta T_e = T_e - T_l = \frac{q^2 E_o^2}{2C_{th}m} \frac{\tau_m \tau_e}{1+\omega^2\tau_m^2} = \frac{q^2\eta P_{in}}{2C_{th}m} \frac{\tau_m \tau_e}{1+\omega^2\tau_m^2} \qquad (1)$$

4    where $m$ is the electron mass, $C_{th}$ is the specific heat of the electron (approximately equal to

5    Boltzmann's constant, $k$), $T_e$ is the electron temperature, $T_l$ is the lattice temperature, $\tau_m$ is the

6    momentum relation time, and $\tau_e$ is the energy relaxation time. The input power $P_{in}$ is related to

7    the radiation field via $P_{in} = E_0^2/2\eta$, where $\eta$ is the intrinsic impedance of the material. An

8    important parameter for sensitivity is $C_{th}$. Its inherently small value results in sizeable values of

9    $T_e$ for small values of $P_{in}$. It is seen that, since the time constant $\tau_m$ is typically on the order of

10   0.1 picoseconds, the high frequency roll-off for the response of the electron gas is about 10 THz.

11

12          To understand the thermionic behavior of the device of FIG. 1, consider the energy

13   diagram in FIG. 2. The important current components are shown which include the

14   recombination component $J_{rb}$ (flow of holes from the emitter), the thermionic emission current

15   (labeled "1") flowing from the n-type modulation doped layer to the quantum well, the

16   thermionic emission current (labeled "2") flowing from the quantum well to the n-type

17   modulation doped layer, and the generation current $J_{gen}$ in the collector which adds electrons to

18   the quantum well and also supplies the hole current flowing to the back junction. The current

19   flow equation is indicated in the figure, in which the recombination is a small current equal to the

20   difference between large emission currents into and out of the quantum well (for zero bias, $J_{rb}=0$

21   and the emission currents are just balanced). In the absence of radiation (with some nominal bias

22   $V_a$ ), the lattice temperature $T_l$ and the electron temperature $T_e$ are equal and $J_{rb}$ represents the

23   dark current in the device. Another significant component is $J_{pb}$, representing thermionic

24   emission over the barrier. The changes in the current $J_{pb}$ represent the output of the detector. The

25   equation that represents this balance of currents is

26
$$J_{rbo}\left[\left(\frac{n_o}{n_o*}\right)^{1/2}e^{\Delta V_b/2V_T}-1\right] = qv_{th}n_o e^{-\varphi_2/kT_e} - qv_{th}\frac{N_c e^{(E_{Fn}-E_c)/kT}}{1+\frac{1}{4}e^{(E_{Fn}-E_c)/kT}}e^{-\varphi_1/kT_l} \qquad (2)$$

27   where the left hand side (LHS) is the recombination current flowing in the emitter as shown in

28   FIG. 2. This is the continuity current written from the viewpoint of the modulation doping. The

1  two terms on the right hand side (RHS) represent the thermionic emission components between

2  the quantum well and the modulation doped layer and both of them contain T in the exponent of

3  the exponential term. However, with the coupling of radiation into the quantum well, the

4  temperature of the quantum well component becomes $T_e$ and the temperature of the component

5  from the modulation doped layer to the quantum well remains at $T_L$. Therefore there is a net

6  thermionic flow from the quantum well to the modulation doped layer. This leads to a

7  decreasing value of $n_o$, which is the electron density in the quantum well. The change in $T_e$ will

8  be small. We may expand this term and obtain the following:

9
$$J_{rbo}\left[\left(\frac{n_o}{n_o*}\right)^{1/2}e^{\Delta V_b/2V_T}-1\right]=qv_{th}n_oe^{-\varphi_2/kT_e}-qv_{th}\frac{N_ce^{(E_{Fn}-E_c)/kT}}{1+\frac{1}{4}e^{(E_{Fn}-E_c)/kT}}e^{-\varphi_1/kT_i}+qv_{th}n_oe^{-\varphi_2/kT_e}\frac{\varphi_2}{kT_L}\frac{\Delta T_e}{T_L}$$

10                                                                          (3)

11

12  We see that the last term is a driving force, which is proportional to the change $\Delta T_e$. We also see

13  from (1), that this change in $T_e$ is proportional to the input power of the received radiation.

14  Therefore the additional term corresponds to R*Pin where R is the responsivity in

15  amps/watt for the basic mechanism of transferring electrons to the modulation doping. Thus the

16  value of R is:

17
$$R=qv_{th}n_oe^{-\varphi_2/kT_e}\frac{\varphi_2}{kT_L}\frac{1}{T_L}\frac{q^2\eta}{2Cm}\frac{\tau_m\tau_e}{1+\omega^2\tau_m^2}\qquad(4)$$

18  The other equation that describes the current flow through the device is

19
$$J_{rb}=J_{rbo}\left[\left(\frac{n_o}{n_o^*}\right)^{1/2}e^{\Delta V_b/2V_T}-1\right]=J_{gen}\qquad(5)$$

20  which simply states that the net current flowing through the device during this process must

21  remain constant since the effect of the radiation is simply to shift the charge internal to the

22  device. The shifting of charge from the well to the sheet region causes $n_o$ to decrease. From

23  equation (5), since $J_{gen}$ is constant, $\Delta V_b$ will increase. The increase in $\Delta V_b$ will cause the current

24  $J_{pb}$ in FIG. 2 to increase. It is this increase in current that represents the net output current of the

25  device and is proportional to the input power of the received radiation. By rearranging (5) and

26  calculating the current $\Delta J_{pb}$, we obtain

$$\Delta J_{pb} = J_{pbco} \left\{ \frac{J_{gen}}{J_{rbo}} - 1 \right\}^2 \frac{n_o^*}{[(C_b + C_d)\Delta V_{bd} - C_d V_{CE}]^2} \frac{R}{qv} P_{in} = R_{eff} P_{in} \qquad (6)$$

The output current is an increase in the collector current that flows in response to the input power $P_{in}$ of the received radiation. Substituting typical numbers yields $R_{eff} \approx 0.05 A/W$. This number is quite reasonable by comparison to typical responsivities for long wavelength infra-red (LWIR) radiation.

An important point should be noted here. The dark current flowing in the system is $J_{gen}$ and this is the generation current across the energy gap of the AlGaAs. This is not the current thermally activated out of a well of extremely low energy. The thermal currents flowing in and out of the well are always in balance even in equilibrium and under bias, and as such they produce no noise. It is only the net dark current $J_{gen}$ that produces noise. This means that the cryogenic cooling will not be required to eliminate the effects of dark current noise. Thus, the detection of the incident radiation occurs at room temperature.

Alternatively, a thyristor structure may be used as a radiation detector. As shown in FIG. 3A, the thyristor structure includes an n-type quantum-well-base bipolar transistor and p-type quantum-well-base bipolar transistor arranged vertically to share a common collector region. The thyristor structure is formed inside a resonant cavity (provided by bottom and top dielectric mirrors) that is adapted to receive electromagnetic radiation in a desired portion of the electromagnetic spectrum. Similar to the operation of the n-type quantum well structure of the quantum-well-base bipolar transistor of FIG. 1, absorbed radiation will empty the p-type quantum well interface of the thyristor, thus accumulating a charge in the p-type modulation doped layer and producing a forward bias $\Delta v_b$ on the p-type quantum well interface barrier, which results in a current flow $I_{nb}$ as shown in FIG. 3B. The current $I_{nb}$ flows over the p-type quantum well interface barrier to the n-type quantum well interface. This current causes charge $Q_n$ to accumulate in the n-type quantum well interface. The accumulated charge $Q_n$ represents the intensity of the received radiation. The operation of the heterojunction-thyristor- based radiation detector is suitable for many imaging applications, including CCD-type imaging applications and active-pixel type imaging applications as described below in detail.

1      The structure of the two thyristor-based pixel elements 101A, 101B is illustrated in FIG.

2   3A.  Note that the general structure of FIG. 3A can be configured to operate as a wide range of

3   electronic devices (e.g., field effect transistors, bipolar transistors) such that these devices can be

4   integrated to form a monolithic optoelectronic integrated circuit as described herein.  The

5   structure includes a bottom dielectric distributed bragg reflector (DBR) mirror 112 formed on a

6   substrate 110.  The bottom DBR mirror 112 typically is formed by depositing pairs of

7   semiconductor or dielectric materials with different refractive indices.  When two materials with

8   different refractive indices are placed together to form a junction, light will be reflected at the

9   junction.  The amount of light reflected at one such boundary is small.  However, if multiple

10   junctions/layer pairs are stacked periodically with each layer having a quarter-wave ($\lambda/4n$)

11   optical thickness, the reflections from each of the boundaries will be added in phase to produce a

12   large amount of reflected light (e.g., a large reflection coefficient) at the particular center

13   wavelength $\lambda_D$.  Deposited upon the bottom DBR mirror 112 is the active device structure which

14   logically consists of two HFET devices. The first of these is a p-channel HFET device 111

15   (referred to herein as PHFET 111) comprising layers 114, 116, 118, and 120.  The PHFET

16   device 111 which has one or more p-type modulation doped quantum well channels and is

17   positioned with the gate terminal on the lower side (i.e. on the bottom DBR mirror 112) and the

18   collector terminal on the upper side. The second of these is an n-channel HFET device 113

19   (referred to herein as NHFET 113) comprising layers 120, 122, 124, and 126.   The NHFET

20   device 113 has one or more n-type modulation doped quantum well channels and is positioned

21   with the gate terminal on the top side and the collector terminal on the lower side which is the

22   collector of the p-channel device.  Therefore a non-inverted N-channel device is stacked upon an

23   inverted p-channel device to form the active device structure.

24

25      The active device layer structure begins with n-type layer(s) 114.  Preferably, n-type

26   layer(s) 114 include at least one layer that enables the formation of ohmic contacts thereto and a

27   heavily doped layer that should not be depleted in any range of operation of the device, i.e. the

28   total doping in this layer should exceed the total doping charge contained in the modulation

29   doped layer of the p-type modulation doped quantum well interface 118 described below.  This

30   layer 114 also serves optically as a small part of the lower waveguide cladding for optical

31   devices realized in this structure.  Note that a majority of the lower waveguide cladding is

1    provided by the lower DBR mirror 112 itself. Deposited on layer 114 is an undoped spacer layer

2    116. Layers 114 and 116 serve electrically as part of the gate of the p-channel HFET 111. In

3    this configuration, layer 114 achieves low contact resistance and layer 116 defines the

4    capacitance of the p-channel HFET 111 with respect to the p-type modulation doped quantum

5    well heterostructure 118. Deposited on layer 116 is a p-type modulation doped quantum well

6    interface 118 that defines one or more quantum wells (which may be formed from strained or

7    unstrained heterojunction materials) spaced apart from a p-type modulation doped layer.

8    Deposited on the p-type modulation doped quantum well interface 118 is an undoped spacer

9    layer 120, which forms the collector of the P-channel HFET device 111. All of the layers grown

10   thus far form the P-channel HFET device 111 with the gate ohmic contact on the bottom.

11

12          Undoped spacer layer 120 forms the collector region of the N-channel HFET device 113.

13   Deposited on layer 120 is an n-type modulation doped quantum well interface 122 that defines

14   one or more quantum wells (which may be formed from strained or unstrained heterojunction

15   materials) spaced apart from an n-type modulation doped layer. Deposited on the n-type

16   modulation doped quantum well interface 122 is an undoped spacer layer 124. Deposited on

17   layer 124 are p-type layer(s) 126. Preferably, the p-type layer(s) 126 include a heavily doped

18   layer that should not be depleted in any range of operation of the device, i.e. the total doping in

19   this layer should exceed the total doping charge contained in the modulation doped layer of the

20   n-type modulation doped quantum well structure 122 described above. In addition, the p-type

21   layer(s) 126 preferably include at least one layer which enables the formation of ohmic contacts

22   thereto. In this configuration, layer(s) 126 achieves low contact resistance and layer 124 defines

23   the capacitance of the n-channel HFET 113 with respect to the n-type modulation doped

24   quantum well interface 122. Layers 126 and 128 serve electrically as part of the gate of the n-

25   channel HFET 113.

26

27          Alternatively, the active device structure may be described as a pair of stacked quantum-

28   well-base bipolar transistors formed on the bottom DBR mirror 112. The first of these is an n-

29   type quantum-well-base bipolar transistor (comprising layers 114, 116, 118, and 120) which has

30   one or more quantum wells spaced apart from a p-type modulation doped layer and is positioned

31   with the emitter terminal on the lower side (i.e. on the mirror as just described) and the collector

1  terminal on the upper side. The second of these is an n-type quantum-well-base bipolar

2  transistor comprising layers 120, 122, 124, and 126. This n-type quantum-well-base bipolar

3  transistor has one or more quantum wells spaced apart from an n-type modulation doped layer

4  and is positioned with the emitter terminal on the top side and the collector terminal on the lower

5  side (which is the collector of the p-type quantum-well-base bipolar transistor). Therefore a non-

6  inverted n-channel device is stacked upon an inverted p-channel device to form the active device

7  structure. In this configuration, the gate terminal of the p-channel HFET device 111 corresponds

8  to the emitter terminal of the p-type quantum-well-base bipolar transistor, the p-type quantum

9  well interface 118 corresponds to the base region of the p-type quantum-well-base bipolar

10  transistor, spacer layer 120 corresponds to the collector region of both the p-type quantum-well-

11  base bipolar transistor and the n-type quantum-well-base bipolar transistor, the n-type quantum

12  well interface 122 corresponds to the base region of the n-type quantum-well-base bipolar

13  transistor, and the gate terminal of the n-channel HFET device 113 corresponds to the emitter

14  electrode of the n-type quantum-well-base bipolar transistor.

15

16  To form a resonant cavity device, a top dielectric mirror 128 is formed over the p-type

17  layer(s) 126 of the device. Incident radiation enters the resonant cavity in a vertical direction

18  through an optical aperture (not shown) in the top surface (or bottom surface) of the device. The

19  optical path length between the bottom DBR mirror and top dielectric mirror preferably

20  represents an integral number of 1/2 wavelengths at the designated wavelength. Preferably, this

21  optical path length is controlled by adjusting the thickness of one or more of the layers

22  therebetween to enable this condition.

23

24  The thyristor-based pixel elements 101A, 101B are adapted to perform an imaging cycle

25  including a Pixel Setup Mode, a Signal Integration Mode, and a Signal Transfer Mode.

26

27  In the Pixel Setup Mode, the n-type modulation doped quantum well interface 122 of the

28  pixel element is emptied of free electrons, thereby forcing the n-type modulation doped quantum

29  well interface 122 into a state of deep depletion. Preferably, this is accomplished by applying a

30  multiphase clock scheme to the anode terminal electrode of the pixel element in a manner similar

31  to the Signal Transfer Mode described below. Such operations clock the charge out of the pixel

1     element via the n-type modulation doped quantum well interface 122. In CCD-type applications,

2     the charge clocked out from a given thyristor-based pixel element (e.g., thyristor device 101A) is

3     clocked into the adjacent thyristor-based pixel element (e.g., thyristor device 101B) utilizing the

4     n-type modulation doped quantum well interface 122 between the adjacent thyristor-based pixel

5     elements as the pathway for charge transfer. An n-channel injector contact that contacts the n-

6     type modulation doped quantum well interface 122 for the last pixel is coupled to circuitry that

7     disposes of the charge read out from the thyristor-based pixel elements in the Pixel Setup Mode.

8     During the initialization operations of Pixel Setup Mode, electronic shutter control circuitry is

9     preferably coupled to the cathode terminal electrode of the thyristor-based pixel element and

10     maintains the cathode terminal electrode in a high impedance state (i.e., in other words the

11     cathode terminal electrode floats) to thereby disable signal accumulation.

12

13     In the Signal Integration Mode, incident radiation is absorbed in the p-type modulation

14     doped quantum well interface 118 of the thyristor-based pixel element. As described above,

15     absorbed radiation will empty the p-type quantum well interface 118, thus accumulating a charge

16     in the p-type modulation doped layer and producing a forward bias $\Delta v_b$ on the p-type quantum

17     well barrier, which results in a current flow $I_{nb}$ as shown in FIG. 3B. The current $I_{nb}$ flows over

18     the p-type barrier to the n-type modulation doped quantum well interface 122 of the thyristor-

19     based pixel element. This current causes charge $Q_n$ to accumulate in the n-type modulation

20     doped quantum well interface 122 of the pixel element. This accumulated charge $Q_n$ represents

21     the intensity of the received radiation over the time period (sometimes referred to as "integration

22     time period) of the Signal Integration Mode. Preferably, such charge-accumulation operations

23     are accomplished by maintaining the voltage level at the anode terminal electrode at a positive

24     voltage (e.g., on the order of three volts). In addition, electronic shutter circuitry coupled to the

25     cathode terminal electrode of the thyristor-based pixel element couples the cathode terminal

26     electrode to ground through a bias resistance (not shown) to enable conduction from the cathode

27     terminal as shown in the potential diagram of FIG. 4B.

28

29     In the Signal Transfer Mode, the charge $Q_n$, which was accumulated in the n-type

30     modulation doped quantum well interface 122 during the previous Signal Integration Mode, is

31     read out from the thyristor-based pixel element. Preferably, this is accomplished by applying a

1 multiphase clock scheme to the anode terminal electrode of the pixel element, which clocks the

2 charge out of the pixel element via the n-type modulation doped quantum well interface 122. In

3 CCD-type applications, the charge clocked out from a given thyristor-based pixel element (e.g.,

4 thyristor device 101A) is clocked into the adjacent thyristor-based pixel element (e.g., thyristor

5 device 101B) utilizing the n-type modulation doped quantum well interface 122 between the

6 adjacent thyristor-based pixel elements as the pathway for charge transfer. An n-channel injector

7 contact that contacts the n-type modulation doped quantum well interface 122 for the last pixel is

8 the output of the CCD-type imaging array and may be amplified directly if desired. A wide

9 variety of multiphase clocking schemes well known in the CCD art (such as 4-phase, 3-phase,

10 pseudo 2-phase, true two phase and virtual phase clocking schemes) may be employed to transfer

11 charge between pixels. Such schemes are described in detail in "Kodak CCD Primer, #KCP-

12 001, CHARGE-COUPLED DEVICE (CCD) IMAGE SENSORS," downloaded from

13 http://www.kodak.com/US/en/digital/pdf/ccdPrimerPart2.pdf on April 24, 2003, herein

14 incorporated by reference in its entirety. In an exemplary 1 ½ phase clocking scheme, a voltage

15 level on the order of 0 volts may be applied to the anode terminal electrode for a given thyristor-

16 based pixel element (e.g., thyristor device 101A) and a voltage level on the order of 1.5 volts

17 may be applied the anode terminal electrode for the next thyristor-based pixel element (e.g.,

18 thyristor 101B), to thereby transfer the stored charge out of the given pixel element and into the

19 next pixel element utilizing the n-type modulation doped quantum well interface 122

20 therebetween as the pathway for charge transfer. Upon completion of the Signal Transfer Mode,

21 the imaging cycle is complete and the operation continues to the Pixel Setup Mode of the next

22 imaging cycle.

23

24      During the Signal Transfer Mode, electronic shutter circuitry coupled to the cathode

25 terminal electrode of the pixel element disables signal accumulation. Preferably, this is

26 accomplished by biasing the cathode terminal electrode of the pixel element such that conduction

27 does not occur from the cathode terminal to the n-type quantum well interface 122 of the pixel

28 element. During the Signal Transfer Mode, it is preferable that the p-type modulation doped

29 quantum well interface 118 of the thyristor-based pixel element be emptied of free holes, thereby

30 forcing the p-type modulation doped quantum well interface 118 into a state of deep depletion.

31 Preferably, this is accomplished by applying a negative clock pulse to the p-channel injector

1 terminal of the pixel element such that the p-type modulation doped quantum well interface is

2 emptied of holes as shown in FIG. 4C. Alternatively, this can be accomplished by holding the

3 potential of the p-channel injector terminal of the pixel element at a constant level and applying a

4 positive voltage pulse to the cathode terminal electrode of the pixel element such that the p-type

5 modulation doped quantum well interface is emptied of holes.

6

7      The epitaxial growth structures described above may be realized with a material system

8 based on group III-V materials (such as a GaAs/AlGaAs). Alternatively, strained silicon

9 heterostructures employing silicon-germanium (SiGe) layers may be used to realize the

10 multilayer structures described herein. FIG. 5 illustrates an exemplary epitaxial growth

11 structure utilizing group III-V materials for realizing the structure of FIG. 3A and the

12 optoelectrical/electrical/optical devices formed from this structure in accordance with the present

13 invention.

14

15      The structure of FIG. 5 can be made, for example, using known molecular beam epitaxy

16 (MBE) techniques. As shown, a first semiconductor layer 1151 of AlAs and a second

17 semiconductor layer 1152 of GaAs are alternately deposited (with preferably at least seven pairs)

18 upon a semi-insulating gallium arsenide substrate 1149 in sequence to form the bottom

19 distributed bragg reflector (DBR) mirror 112. The number of AlAs layers will preferably always

20 be one greater than the number of GaAs layers so that the first and last layers of the mirror are

21 shown as layer 1151. In the preferred embodiment the AlAs layers 1151 are subjected to high

22 temperature steam oxidation to produce the compound $Al_xO_y$ so that a mirror will be formed at

23 the designed center wavelength. This center wavelength is selected such that all of the resonant

24 wavelengths for the various cavities of the array will be subject to high reflectivity. Therefore

25 the thicknesses of layers 1151 and 1152 in the mirror are chosen so that the final optical

26 thickness of GaAs and $Al_xO_y$ are one quarter wavelength of the center wavelength $\lambda_D$.

27 Alternatively the mirrors could be grown as alternating layers of one quarter wavelength

28 thickness of GaAs and AlAs at the designed wavelength so that the oxidation step is not used. In

29 that case, many more pairs are required (with typical numbers such as 22 pairs) to achieve the

30 reflectivity needed for efficient lasing.

31

1    Deposited upon the mirror is the active device structure which consists of two HFET

2    devices. The first of these is the p-channel HFET (PHFET) 111 (see Fig. 3A), which has one or

3    more p-type modulation doped quantum wells and is positioned with the gate terminal on the

4    bottom (i.e. on the mirror 112 just described) and the collector terminal above. The second of

5    these is an n-channel HFET (NHFET) 113, which has one or more n-type modulation doped

6    quantum wells and is positioned with the gate terminal on top and the collector terminal below.

7    The collector region of the NHFET device 113 also functions as the collector region of the

8    PHFET device 111. However, the collector terminal of the NHFET device 113 is a p-type

9    contact to p-type quantum well(s) disposed below (above) the collector region, while the

10   collector terminal of the PHFET device 111 is a n-type contact to n-type quantum well(s)

11   disposed above the collector region. Therefore a non-inverted n-channel device is stacked upon

12   an inverted p-channel device to form the active device structure.

13

14   The active-device layer structure begins with layer 1153 of N+ type GaAs that enables

15   the formation of ohmic contacts thereto (for example, when contacting to the cathode terminal of

16   a thyristor device, the gate terminal of an inverted p-channel HFET device, the sub-collector

17   terminal of an n-channel HFET device, or the emitter terminal of a p-type quantum-well-base

18   bipolar device). Layer 1153 has a typical thickness of 1000-3000 Å and a typical n-type doping

19   of $3.5 \times 10^{18}$ cm$^{-3}$. Deposited on layer 1153 is layer 1154 of n-type $Al_{x1}Ga_{1-x1}As$ with a typical

20   thickness of 500-3000 Å and a typical doping of $1 \times 10^{17}$ cm$^{-3}$. The parameter x1 is preferably in

21   the range between 70% and 80% (for example, on the order of 70%) for layer 1154. This layer

22   serves as part of the PHFET gate and optically as a small part of the lower waveguide cladding

23   of the device. Note that a majority of the lower waveguide cladding for waves propagating in the

24   guide formed by the optically active region of the device is provided by the lower DBR mirror

25   itself. The lower DBR mirror causes the light to be guided partially as a dielectric waveguide

26   and partially as a mirror waveguide. Next are 4 layers (1155a, 1155b, 1155c, and 1155d) of

27   $Al_{x2}Ga_{1-x2}As$. These 4 layers (collectively, 1155) have a total thickness about 380-500 Å and

28   where x2 is about 15%. The first layer 1155a is about 60-80 Å thick and is doped N+ type in the

29   form of delta doping. The second layer 1155b is about 200-300 Å thick and is undoped. The

30   third layer 1155c is about 80 Å thick and is doped P+ type in the form of delta doping. The

31   fourth layer 1155d is about 20-30 Å thick and is undoped to form a spacer layer. This layer

1 forms the lower separate confinement heterostructure (SCH) layer for the laser, amplifier and

2 modulator devices. The N+ doped GaAs layer 1153, the n-type AlGaAs layer 1154 and n-type

3 AlGaAs layer 1155a correspond to the n-type layer(s) 114 of FIG. 3A, and the undoped AlGaAs

4 layer 1155b corresponds to the undoped spacer layer 116 of FIG. 3A.

5

6 The next layers define the quantum well(s) that form the inversion channel(s) during

7 operation of the PHFET 111. For a strained quantum well, this includes a spacer layer 1156 of

8 undoped GaAs that is about 10-25 Å thick and then combinations of a quantum well layer 1157

9 that is about 40-80 Å thick and a barrier layer 1158 of undoped GaAs. The quantum well layer

10 1157 may be comprised of a range of compositions. In the preferred embodiment, the quantum

11 well is formed from an $In_{0.2}Ga_{0.8}AsN$ composition with the nitrogen content varying from 0% to

12 5% depending upon the desired natural emission frequency. Thus, for a natural emission

13 frequency of .98$\mu$m, the nitrogen content will be 0%; for a natural emission frequency of 1.3$\mu$m,

14 the nitrogen content will be approximately 2%; and for a natural emission frequency of 1.5$\mu$m,

15 the nitrogen content will be approximately 4-5%. The well barrier combination will typically be

16 repeated (for example, three times as shown), however single quantum well structures may also

17 be used. Unstrained quantum wells are also possible. Following the last barrier of undoped

18 GaAs is a layer 1159 of undoped $Al_{x2}Ga_{1-x2}As$ which forms the collector of the PHFET device

19 111 and is about 0.5$\mu$m in thickness. All of the layers grown thus far form the PHFET device

20 111 with the gate contact on the bottom. The layers between the P+ AlGaAs layer 1155c and the

21 last undoped GaAs barrier layer 1158 correspond to the p-type modulation doped heterojunction

22 quantum well structure 118 of FIG. 3A. Undoped AlGaAs layer 1159 corresponds to the

23 undoped spacer layer 120 of FIG. 3A.

24

25 Layer 1159 also forms the collector region of the NHFET device 113. Deposited on layer

26 1159 are two layers (collectively 1160) of undoped GaAs of about 200-250 Å total thickness,

27 which form the barrier of the first n-type quantum well. Layer 1160 is thicker than the normal

28 barrier layer of about 100 Å because it accommodates the growth interruption to change the

29 growth temperature from 610° C (as required for optical quality $Al_{x2}Ga_{1-x2}As$ layers) to about

30 530°C for the growth of InGaAs. Therefore layer 1160 includes a single layer 1160a of about

31 150 Å and a barrier layer 1160b of about 100 Å. The next layer 1161 is the quantum well of

1      $In_{0.2}Ga_{0.8}As$, which is undoped and about 40-80 Å in thickness. It is noted that the n-type

2      quantum well layer 1161 need not be of the same formulation as the p-type quantum well layer

3      1157. The barrier layer 1160b of 100 Å and quantum well layer 1161 may be repeated, e.g.,

4      three times. Then there is a barrier layer 1162 of about 10-30 Å of undoped GaAs which

5      accommodates a growth interruption and a change of growth temperature. Next there are four

6      layers (collectively 1163) of $Al_{x2}Ga_{1-x2}As$ of about 300-500 Å total thickness. These four layers

7      (1163) include a spacer layer 1163a of undoped $Al_{x2}Ga_{1-x2}As$ that is about 20-30 Å thick, a

8      modulation doped layer 1163b of N+ type doping of $Al_{x2}Ga_{1-x2}As$ (with doping about $3.5 \times 10^{18}$

9      $cm^{-3}$) that is about 80 Å thick, a spacer layer 1163c of undoped $Al_{x2}Ga_{1-x2}As$ that is about 200-

10      300 Å thick, and a P+ type delta doped layer 1163d of $Al_{x2}Ga_{1-x2}As$ (with doping about $3.5 \times 10^{18}$

11      $cm^{-3}$) that is about 60-80 Å in thickness. Layers 1163b and 1163d form the top plate and bottom

12      plate of a parallel plate capacitor which forms the field-effect input to all active devices. The

13      doping species for layer 1163d is preferably carbon (C) to ensure diffusive stability. In contrast

14      to layer 1163b which is always depleted, layer 1163d should never be totally depleted in

15      operation. For the optoelectronic device operation, layer 1163 is the upper SCH region. The

16      layers between the undoped GaAs barrier layer 1160a and the N+ AlGaAs layer 1163b

17      correspond to the n-type modulation doped heterojunction quantum well structure 122 of FIG.

18      3A. Undoped AlGaAs layer 1163c corresponds to the undoped spacer layer 124 of FIG. 3A.

19

20      One or more layers (collectively 1164) of p-type $Al_{x1}Ga_{1-x1}As$ are deposited next to form

21      part of the upper waveguide cladding for the laser, amplifier and modulator devices. Note that a

22      majority of the upper waveguide cladding for waves propagating in the guide formed by the

23      optically active region of the device is provided by the upper dielectric mirror itself. The upper

24      dielectric mirror causes the light to be guided partially as a dielectric waveguide and partially as

25      a mirror waveguide. Preferably, layer 1164 has a thickness on the order of 500-1500 Å, and

26      includes a first thin sublayer 1164a that is 10-20 Å thick and has a P+ doping of $10^{19}$ $cm^{-3}$ and a

27      second sublayer 1164b that is 700 Å thick and has a P doping of $1 \times 10^{17} - 5 \times 10^{17}$ $cm^{-3}$. The

28      parameter x1 of layer 1164 is preferably about 70%. Deposited next is an ohmic contact layer

29      1165 (which may comprise a single layer of GaAs or a combination of GaAs (1165a) and

30      InGaAs (1165b) as shown). Layer 1165 is about 50-100 Å thick and is doped to a very high

31      level of P+ type doping (about $1 \times 10^{20}$ $cm^{-3}$) to enable formation of ohmic contacts thereto (for

1    example, when contacting to the anode terminal of a thyristor device). The p-type layers 1163b,

2    1164a, 1164b, 1165a and 1165b correspond to the p-type layer(s) 126 of FIG. 3A.

3

4          Alternatively, the active device structure may be described as a pair of stacked quantum-

5    well-base bipolar transistors formed on the bottom DBR mirror (layers 1151/1152). The first of

6    these is an p-type quantum-well-base bipolar transistor (comprising layers 1153 through 1159)

7    which has one or more p-type modulation doped quantum wells and is positioned with the

8    emitter terminal on the lower side (i.e. on the bottom mirror as just described) and the collector

9    terminal on the upper side. The second of these is an n-type quantum-well-base bipolar

10    transistor (comprising layers 1159 through 1165b) which has one or more n-type modulation

11    doped quantum wells and is positioned with the emitter terminal on the top side and the collector

12    terminal on the lower side which is the collector of the p-type quantum-well-base bipolar

13    transistor. Therefore a non-inverted n-channel device is stacked upon an inverted p-channel

14    device to form the active device structure. In this configuration, the cathode terminal of the

15    thyristor device corresponds to the emitter electrode of the p-type quantum-well-base bipolar

16    transistor, the p-type quantum well structure (layers 1155c though 1158) corresponds to the base

17    region of the p-type quantum-well-base bipolar transistor, spacer layer 1159 corresponds to the

18    collector region of both the p-type quantum-well-base bipolar transistor and the n-type quantum-

19    well-base bipolar transistor, the n-type quantum well structure (layers 1160a through 1163b)

20    corresponds to the base region of the n-type quantum-well-base bipolar transistor, and the anode

21    terminal of the thyristor device correspond to the emitter electrode of the n-type quantum-well-

22    base bipolar transistor.

23

24          To form a resonant cavity device, a top dielectric mirror is formed over the top p-type

25    layer 1165b. Incident radiation enters the resonant cavity in a vertical direction through an

26    optical aperture (not shown) in the top surface (or bottom surface) of the device. The optical

27    path length between the bottom DBR mirror and top dielectric mirror preferably represents an

28    integral number of 1/2 wavelengths at the designated wavelength. Preferably, this optical path

29    length is controlled by adjusting the thickness of one or more of the layers therebetween to

30    enable this condition.

31

1    The structure of FIG. 5 may also be used to realize various optoelectronic devices,

2    including transistor devices (such as n-channel HFET devices, p-channel HFET devices, n-type

3    quantum-well-base bipolar transistors and p-type quantum-well-base bipolar transistors), and

4    other optoelectronic and waveguide devices. Such devices are described in detail in U.S. Patent

5    Application No. 10/323,388, filed on December 19, 2002; and U.S. Patent Application No.

6    10/340,942, filed on January 13, 2003; incorporated by reference above in their entireties.

7

8    FIGS. 6A, 6B1, 6B2 and 6C illustrate schematic views of an exemplary realization of two

9    thyristor-based pixel elements. The structure of layers 1149 through 1165b as described above

10   with respect to FIG. 5 is provided. To connect to the anode of the thyristor-based pixel elements,

11   alignment marks (not shown) are defined by etching, and then a layer of $Si_3N_4$ or $Al_2O_3$ or other

12   suitable dielectric (not shown) is deposited to act as protection for the surface layer and as a

13   blocking layer for subsequent ion implants. The refractory anode terminals 136A and 136B of

14   the thyristor-based pixel elements are deposited and defined preferably via liftoff of metal layer

15   610.

16

17   Then mesas are formed to define the imaging areas for the pixel elements of the array.

18   The imaging area for each given pixel element (labeled 620a for pixel element A and 620b for

19   pixel element B) is disposed adjacent the anode terminal metal layer 610 for the given pixel

20   element as shown in FIGS. 6A and 6B1. Preferably, the pixel element mesas are formed by

21   etching down to (or near) p+-type layer 1163d.

22

23   In conjunction with the formation of the pixel element mesas, an ion implant 170 of n+-

24   type is performed into the portion of the mesa that is not covered by the anode metal layer as

25   shown in FIG. 6B1. The purpose of n+-type implants 170 is to move the threshold of the

26   implanted region 191 of the n-type modulation doped quantum well interface of each pixel

27   element to a normally-on condition (i.e., on condition with zero anode voltage). Note that the

28   region 192 of the n-type modulation doped quantum well interface under the anode metal layer,

29   which is not subject to the n+-type implants 170, has a threshold with a normally-off condition

30   (i.e., off condition with zero anode voltage). In this configuration, the implanted region 191 acts

1   as a charge storage region and the region 192 acts as a voltage-controlled barrier as described

2   below in more detail.

3

4   In conjunction with the formation of the pixel element mesas, interpixel transfer regions

5   622 are formed between the pixel elements of the array as shown in FIGS. 6A and 6B1. The n-

6   type modulation doped interface in the interpixel transfer regions 622 is used for charge transfer

7   between adjacent pixel elements as described herein in detail. Preferably, an ion implant 171 of

8   n+ type is performed using a photomask that is aligned to the alignments marks to implant n-type

9   ions into the n-type modulation doped quantum well interface of the interpixel transfer regions

10  622. The n+-type ion implants 171 provide for improved charge transfer efficiency as described

11  below.

12

13  In addition, an ion implant 172 of p+-type is performed using a photomask that is aligned

14  to the alignments marks, to thereby form contacts to the p-type modulation doped quantum well

15  interface for each pixel element as shown in FIG. 6B2. During this operation, mesas are formed

16  by etching preferably down to the undoped spacer layer 1159. The resulting mesas are then

17  subject to P+ ion implant 172. The implant 172 is subsequently metallized as described below to

18  form a p-channel injector terminal 139 as shown in FIGS. 6A and 6B2.

19

20  Connection of the cathode of the thyristor-based pixel elements is made by etching down

21  to the n-type ohmic contact layer 1153. The exposed portion of the n-type ohmic contact layer

22  1153 is subsequently metallized as described below to form a cathode terminal 140 as shown in

23  FIG. 6A.

24

25  Next the thyristor-based pixel elements are subjected to a rapid thermal anneal (RTA) of

26  the order of 900°C or greater to activate all implants. Then the thyristor-based pixel elements are

27  isolated from one another by etching down to the semi-insulating substrate 1149. Oxygen

28  implants may be used to create high resistance regions below the implants. In addition, the AlAs

29  layers 1151 (and other layers with large aluminum percentages) are oxidized to achieve

30  passivation, isolation and the bottom DBR mirror.

31

1    The next step in the fabrication is the deposition (preferably via lift off) of metal

2    contacts. These contacts come in three forms. One is a metal layer 612 (preferably comprising

3    an n-type Au alloy metal such as AuGe/Ni/Au) deposited on the n-type contact layer 1153 to

4    form the cathode terminal electrode 140 as seen in FIG. 6A. The second is a metal layer 614

5    (preferably comprising a p-type Au metal alloy such as AuZn/Cr/Au) deposited on the P+ type

6    implant 172 to form the p-channel injector terminal electrode 139 as shown in FIGS. 6A and

7    6B2. The third is the metal layer 616 (preferably comprising an n-type Au alloy metal such as

8    AuGe/Ni/Au) deposited on the N+ type implant 171 to form an n-channel injector terminal

9    electrode for one or more thyristor-based pixel elements. In the exemplary configuration shown,

10   the pixel elements share a common p-channel injector terminal and a common cathode terminal

11   as best shown in FIG. 6A. Note that an n-channel injector terminal is preferably formed for the

12   last pixel of the array. This n-channel injector terminal is the output of the array and may be

13   amplified directly if desired.

14

15   To form thyristor-based pixels suitable for vertical optical injection into a resonant

16   vertical cavity, a top dielectric mirror is added to the structure preferably by the deposition of

17   one or more dielectric layer pairs 196/197 (one pair shown in FIG. 6B). Such dielectric pairs

18   typically comprise $SiO_2$ and a high refractive index material such as GaAs, Si, or GaN,

19   respectively.

20

21   Note that optoelectronic devices (e.g., lasers, optical detectors, optical modulators, optical

22   amplifiers) include n-type ion implants (not shown) into the top contact layer 1165b. An optical

23   aperture is defined by the separation between these implants. These implants create a p-n

24   junction in the layers between the n-type quantum well(s) and the surface, and the aperture

25   between the implants defines the region in which the current may flow, and therefore the

26   optically active region of the device. The current cannot flow into the n-type implanted regions

27   because of the barrier to current injection. In addition, to form a device suitable for in-plane

28   optical injection into a resonant vertical cavity and/or in-plane optical emission from the resonant

29   vertical cavity, a diffraction grating (not shown), as described in more detail in U.S. Patent

30   6,021,243, incorporated by reference above in its entirety) is added to the structure as described

31   above.

1

2      Also note that the operations described above to realize a thyristor device (and other

3   optoelectronic devices) from the multilayer structure of FIG. 5 are readily adaptable to realize a

4   wide variety of electronic devices (such as HFET transistors, quantum-well-base transistors, etc,

5   and associated logic and signal processing circuitry) from the multilayer structure of FIG. 5.

6

7      The thyristor-based pixel elements of FIGS. 6A - 6C are adapted to perform an imaging

8   cycle including a Pixel Setup Mode, a Signal Integration Mode, and a Signal Transfer Mode.

9

10      In the Pixel Setup Mode, the n-type modulation doped quantum well interface (layers

11   1160a - 1163b) of the thyristor-based pixel elements are emptied of free electrons, thereby

12   forcing the n-type modulation doped quantum well interface into a state of deep depletion.

13   Preferably, this is accomplished by applying a multiphase clock scheme to the anode terminal

14   electrodes 136A, 136B, ... of the pixel elements in a manner similar to the Signal Transfer Mode

15   described below. Such operations transfers charge between pixel elements via the n-type

16   modulation doped quantum well interface (layers 1160a - 1163c) of the interpixel transfer region

17   therebetween. An n-channel injector contact that contacts the n-type modulation doped quantum

18   well interface (layers 1160a - 1163c) for the last pixel is coupled to circuitry that disposes of the

19   charge read out from the thyristor-based pixel elements in the Pixel Setup Mode. During the

20   initialization operations of Pixel Setup Mode, electronic shutter control circuitry is preferably

21   coupled to the common cathode terminal electrode 140 of the thyristor-based pixel elements and

22   maintains the common cathode terminal electrode 140 in a high impedance state (i.e., in other

23   words the cathode terminal electrode floats) to thereby disable signal accumulation.

24

25      In the Signal Integration Mode, incident radiation is absorbed in the p-type modulation

26   doped quantum well interface (layers 1155c - 1158) of the thyristor-based pixel elements. As

27   described above, absorbed radiation will empty the p-type quantum well interface, thus

28   accumulating a charge in the p-type modulation doped layer and producing a forward bias $\Delta v_b$ on

29   the p-type quantum well interface barrier, which results in a current flow $I_{nb}$ as shown in FIG.

30   3B. The current $I_{nb}$ flows over the p-type QW barrier to the n-type modulation doped quantum

31   well interface. This current causes charge $Q_n$ to accumulate in the n-type modulation doped

1    quantum well interface. This accumulated charge $Q_n$ represents the intensity of the received

2    radiation at the given pixel element over the time period (sometimes referred to as "integration

3    time period) of the Signal Integration Mode. Preferably, such charge-accumulation operations

4    are accomplished by maintaining the voltage level at the anode terminal electrodes 136A, 136B,

5    ... of the thyristor-based pixel elements at a positive voltage (e.g., on the order of three volts). In

6    addition, electronic shutter circuitry coupled to the common cathode terminal electrode 140

7    couples the common cathode terminal electrode 140 to ground through a bias resistance (not

8    shown) to enable conduction from the common cathode terminal 140 as shown in the potential

9    diagram of FIG. 4B.

10

11    In the Signal Transfer Mode, the charge $Q_n$, which was accumulated in the n-type

12    modulation doped quantum well interface during the previous Signal Integration Mode, is read

13    out from the thyristor-based pixel elements. Preferably, this is accomplished by applying a

14    multiphase clock scheme to the anode terminal electrodes 136A, 136B, ... of the pixel elements,

15    which clocks the charge out of the pixel elements via the n-type modulation doped quantum well

16    interface. In CCD-type applications, the charge clocked out from thyristor-based pixel element

17    A is clocked into the adjacent thyristor-based pixel element B utilizing the n-type modulation

18    doped quantum well interface (layers 1160a - 1163c) of the interpixel transfer regions 622

19    therebetween as the pathway for charge transfer. These operations are repeated over the pixel

20    elements of the CCD-type array. An n-channel injector contact that contacts the n-type

21    modulation doped quantum well interface for the last thyristor-based pixel element is the output

22    of the CCD imaging array and may be amplified directly if desired. Upon completion of the

23    Signal Transfer Mode, the imaging cycle is complete and the operation continues to the Pixel

24    Setup Mode of the next imaging cycle.

25

26    As previously described, a wide variety of multiphase clocking schemes well known in

27    the CCD art (such as 4-phase, 3-phase, pseudo 2-phase, true two phase and virtual phase

28    clocking schemes) may be employed to transfer charge between pixels. Such schemes are

29    described in detail in "Kodak CCD Primer, #KCP-001, CHARGE-COUPLED DEVICE (CCD)

30    IMAGE SENSORS," downloaded http://www.kodak.com/US/en/digital/pdf/ccdPrimerPart2.pdf

1 on April 24, 2003, incorporated by reference above in its entirety. In an exemplary 1 ½ phase

2 clocking scheme, a voltage level on the order of 0 volts may be applied to the anode terminal

3 electrode for a given thyristor-based pixel element (e.g., pixel element A) and a voltage level on

4 the order of 1.5 volts may be applied the anode terminal electrode for the next thyristor-based

5 pixel element (e.g., pixel element B), to thereby transfer the stored charge out of the given pixel

6 element and into the next pixel element utilizing the n-type modulation doped quantum well

7 interface as the pathway for charge transfer. This 1 ½ phase clocking scheme relies on the

8 potential differences between the implanted region 191 and the voltage-controlled barrier region

9 192 within the n-type modulation doped quantum well interface of the pixel elements as

10 described above and shown in FIG. 6B. In this configuration, during charge transfer operations,

11 charge is accumulated in the thyristor-based pixel element A by applying a reverse-bias between

12 the anode terminals 136A, 136B, respectively, as shown in potential profile labeled "Charge

13 Accumulation" in FIG. 6C. A reverse-bias is also applied between the anode terminal 136A and

14 the anode terminal for the previous pixel element (not shown), respectively. In this bias state,

15 the barrier regions 192-A and 192-B act as a barrier to the flow of charge between the pixel

16 elements. The accumulated charge is transferred from the implanted region 191-A for pixel

17 element A to the implanted region for the implanted region 191-B for pixel element B by

18 applying a forward-bias between the anode terminals 136A, 136B, respectively, as shown in

19 potential profile labeled "Charge Transfer" in FIG. 6C. In this bias state, the potential barrier

20 provided by the barrier region 192-B is eliminated (or substantially reduced) such that charge

21 flows freely from the implanted region 191-A for pixel element A to the implanted region for the

22 implanted region 191-B via the n-type modulation doped quantum well interface therebetween.

23 These charge transfer operations are repeated over the pixel elements of the CCD-type array to

24 read out the charge accumulated in the thyristor-based pixel elements in a sequential fashion.

25

26      During the charge transfer operations, the relative voltage difference supplied to the

27 anode terminals of the adjacent pixels is applied to the n-type ion implanted interpixel transfer

28 regions 622 that is disposed between the pixel mesas as shown in FIGS. 6A and 6B1.

29 Preferably, the length of the resistor (i.e., the spacing between pixel mesas) is selected to

30 maximize the charge velocity between pixels which therefore maximizes transfer efficiency.

31 More specifically, in order to maximize transfer efficiency, it is necessary to maximize the drift

1    current between pixels. More specifically, the drift current is given by $J = q * v * n$, where $v$ is

2    the carrier velocity, $q$ is the electronic charge, and $n$ is the carrier density. The drift current is

3    maximized by obtaining a maximum value of $v$ (which is achieved by selecting the appropriate

4    resistor length) and by obtaining a maximum value of $n$ (which is obtained by the n+-implants

5    170 of the interpixel transfer regions 622 as shown in FIG. 6B1).

6

7           During the Signal Transfer Mode, electronic shutter circuitry coupled to the cathode

8    terminal electrode 140 of the pixel elements disables signal accumulation. Preferably, this is

9    accomplished by biasing the cathode terminal electrode of the pixel elements such that

10   conduction does not occur from the cathode terminal to the n-type quantum well interface (layers

11   1160a - layers 1163b) of the thyristor-based pixel elements. During the Signal Transfer Mode, it

12   is preferable that the p-type modulation doped quantum well interface (layers 1155c - 1158) of

13   the thyristor-based pixel elements are emptied of free holes, thereby forcing the p-type

14   modulation doped quantum well interface into a state of deep depletion. Preferably, this is

15   accomplished by applying a negative clock pulse to the p-channel injector terminal 139 of the

16   pixel elements such that the p-type modulation doped quantum well interface is emptied of holes

17   as shown in FIG. 4C. Alternatively, this can be accomplished by holding the potential of the p-

18   channel injector terminal 139 of the pixel elements at a constant level and applying a positive

19   voltage pulse to the cathode terminal electrode 140 of the pixel elements such that the p-type

20   modulation doped quantum well interface is emptied of holes.

21

22          The thyristor-based pixel elements as described above may be utilized in a variety of

23   imaging arrays. For example, FIG. 7A illustrates a full-frame-type imaging array wherein the

24   thyristor-based pixel elements are arranged in columns of CCD-type elements. The last

25   pixel/CCD in each column is coupled to a horizontal CCD shift register. In this architecture, the

26   charge stored in the pixel/CCD elements is transferred vertically to the horizontal CCD shift

27   register for output therefrom.

28

29          FIG. 7B illustrates an interline-type imaging array wherein the thyristor-based pixel

30   elements are arranged in columns. The pixels of a given column are electrically coupled to CCD

31   registers to form a vertical pixel array. The last CCD register of each vertical pixel array is

1    coupled to a horizontal CCD shift register. In this architecture, the charge stored in the pixel

2    elements of a given vertical pixel array is transferred to the corresponding CCD registers. The

3    charge stored in the CCD registered is then transferred to the horizontal CCD shift register for

4    output therefrom.

5

6          Note that the horizontal CCD shift register of FIG. 7A and the vertical CCD shift register

7    and horizontal CCD shift register of FIG. 7B may be realized by thyristor-based CCD elements

8    similar to those described above with respect to FIGS. 6A - 6C, which are adapted to perform the

9    CCD-type charge transfer operations as described herein. These elements do not perform

10   imaging operations. Therefore, the common p-channel injector terminal 139 and the common

11   cathode terminal 140 may be omitted.

12

13

14          Turning now to FIGS. 8A-8C, the thyristor-based pixel element can also be used in an

15   active-pixel-type imaging array. As shown in FIG. 8A, the thyristor-based pixel element 801

16   operates in conjunction with a transfer gate 803. The thyristor-based pixel element 801 is

17   realized from the multilayer structure of FIG. 5 in the manner described above. The transfer gate

18   803 is realized from the multilayer structure of FIG. 5 in a manner similar to that described

19   above with respect to the thyristor-based pixel element; however, the metal layer 610 is patterned

20   to substantially cover the mesa that forms the transfer gate 803 as shown. In addition, the

21   threshold adjusting implant 171 is omitted such that the transfer gate 803 operates in a normally-

22   off condition. The thyristor-based pixel element 801 is adapted to perform an imaging cycle

23   including a Pixel Setup Mode, a Signal Integration Mode, and a Signal Transfer Mode as

24   described below.

25

26          In the Pixel Setup Mode, the n-type modulation doped quantum well interface (layers

27   1160a - 1163b) of the thyristor-based pixel element 801 is emptied of free electrons, thereby

28   forcing the n-type modulation doped quantum well interface into a state of deep depletion.

29   Preferably, this is accomplished by applying a multiphase clock scheme to the anode terminal

30   electrode 136 of the pixel element and the gate terminal electrode 141 of the transfer gate 803 in

31   a manner similar to the Signal Transfer Mode described below. Such operations transfer charge

1  from the pixel element to the n-channel injector terminal 142 of the transfer gate 803. The n-

2  channel injector terminal 142 is coupled to circuitry that disposes of the charge read out from the

3  thyristor-based pixel element in the Pixel Setup Mode. This operation, which is depicted by the

4  potential diagram of FIG. 4A, puts the n-type modulation doped quantum well interface of the

5  thyristor-based pixel element 801 into a non-steady state of depletion (devoid of electrons),

6  which will eventually be changed to a steady state of electrons by thermal processes during the

7  signal integration mode. During the initialization operations of Pixel Setup Mode, electronic

8  shutter control circuitry is preferably coupled to the cathode terminal electrode 140 of the

9  thyristor-based pixel element and maintains the cathode terminal electrode 140 in a high

10  impedance state (i.e., in other words the cathode terminal electrode floats) to thereby disable

11  signal accumulation.

12

13      In the Signal Integration Mode, incident radiation is absorbed in the p-type modulation

14  doped quantum well interface (layers 1155c - 1158) of the thyristor-based pixel element 801. As

15  described above, absorbed radiation will empty the p-type quantum well, thus accumulating a

16  charge in the p-type modulation doped layer and producing a forward bias $\Delta v_b$ on the p-type

17  quantum well barrier, which results in a current flow $I_{nb}$ as shown in FIG. 3B. The current $I_{nb}$

18  flows over the p-type QW barrier to the n-type modulation doped quantum well interface of the

19  thyristor-based pixel element 801. This current causes charge $Q_n$ to accumulate in the n-type

20  modulation doped quantum well interface. This accumulated charge $Q_n$ represents the intensity

21  of the received radiation at the pixel element over the time period (sometimes referred to as

22  "integration time period) of the Signal Integration Mode. Preferably, such charge-accumulation

23  operations are accomplished by maintaining the voltage level at both the anode terminal

24  electrode 136 of the pixel element 801 and the gate terminal electrode 141 of the transfer gate

25  803 at a positive voltage (e.g., on the order of three volts). In addition, the cathode terminal

26  electrode 140 is coupled to ground through a bias resistance (not shown) to enable conduction

27  from the cathode terminal 140 as shown in the potential diagram of FIG. 4B.

28

29      In the Signal Transfer Mode, the charge $Q_n$, which was accumulated in the n-type

30  modulation doped quantum well interface during the previous Signal Integration Mode, is read

31  out from the thyristor-based pixel element 801. Preferably, this is accomplished by applying a

1    reverse-bias between the anode terminal electrode 136 and the gate electrode 141 of the transfer

2    gate 803 such that the potential barrier provided by the n-type quantum well interface of the

3    transfer gate 803 is substantially lowered as shown in the potential profile labeled "Charge

4    Transfer" in FIG. 8B. The charge stored in the storage region of the pixel element 801 flows

5    through the n-type modulation doped quantum well interface of the transfer gate 803 and output

6    from the transfer gate 803 by an n-channel injector terminal electrode 142. The electrode 142 is

7    coupled to the n-type modulation doped quantum well interface of the transfer gate 803 via an

8    n+-type implant 170.

9

10    During the Signal Transfer Mode, electronic shutter circuitry coupled to the cathode

11    terminal electrode of the pixel elements disables signal accumulation. Preferably, this is

12    accomplished by biasing the cathode terminal electrode of the pixel elements such that

13    conduction does not occur from the cathode terminal to the n-type quantum well interface (layers

14    1160a - layers 1163b) of the thyristor-based pixel elements. During the Signal Transfer Mode, it

15    is preferable that the p-type modulation doped quantum well interface (layers 1155c - 1158) of

16    the thyristor-based pixel elements 801 are emptied of free holes, thereby forcing the p-type

17    modulation doped quantum well interface into a state of deep depletion. Preferably, this is

18    accomplished by applying a negative clock pulse to the p-channel injector terminal 139 of the

19    pixel element 801 such that the p-type modulation doped quantum well interface is emptied of

20    holes as shown in FIG. 4C. Alternatively, this can be accomplished by holding the potential of

21    the p-channel injector terminal 139 of the pixel element at a constant level and applying a

22    positive voltage pulse to the cathode terminal electrode 140 of the pixel element such that the p-

23    type modulation doped quantum well interface is emptied of holes.

24

25    The thyristor-based pixel element 801 and transfer gate 803 form a pixel 805 of the

26    active-pixel array. The pixels 805 are typically arranged as a linear array as shown in FIG. 8C.

27    The output electrode 142 of the transfer gate 803 of each pixel is electrically coupled to a

28    corresponding output amplifier 807. The output amplifiers 807 of a given linear pixel array are

29    electrically coupled to a common output line 809. In this architecture, the charge stored in the

30    pixel elements of a given linear pixel array are selectively output (one at a time) to the

1    corresponding output amplifier 807 for supply to S/H buffer 811 and readout circuitry 813 via

2    the common output line 809 as shown.

3

4         In the exemplary embodiments described above, the vertical dimension of the resonant

5    cavity for each pixel element corresponds to the desired wavelength of electromagnetic energy

6    that is to be absorbed therein as part of the image sensing operations of the device. In alternate

7    embodiments, the vertical dimensions of the resonant cavities of the pixel elements can vary

8    such that they correspond to different wavelengths of electromagnetic energy. For example,

9    some of the pixel elements can correspond to a first wavelength in one of the short-infrared

10   region (SWIR; 1-3 μm), the mid-infrared region (MWIR; 3-5 μm), the long-infrared region

11   (LWIR; 8-12 μm); and the very-long-infrared region (VLWIR; > 12 μm), while other pixel

12   elements correspond to a second wavelength in another of the these regions. This can be

13   accomplished through the use of subtractive epitaxy of one or more spacer layers formed

14   between the top and bottom mirrors that define the cavity as set forth in U.S. Application No.

15   10/627,043, filed on July 25, 2003, herein incorporated by reference in its entirety. In this

16   configuration, the pixel elements will preferentially absorb particular components of the

17   spectrum. This capability enables multi-spectral imaging. Such multi-spectral response can also

18   be integrated into the pixel element itself. For example, assuming the spectral response of the

19   quantum well structures are broad enough (which can be accomplished by adjusting the width of

20   the quantum wells of such structures), the pixel elements can be divided into sections (for

21   example, 3 in a row, side-by-side, staggered, etc) to perform imaging whereby the sections of the

22   pixel correspond to different wavelengths.

23

24        Also note that detection of energy in the long-infrared (LWIR) region via intersubband

25   absorption requires that the incident energy propagate in a direction such that the electric field is

26   normal to the quantum wells of the pixel element. This constraint stems from the quantum

27   selection rule. In practice, this constraint is not satisfied due to a number of factors, including

28   strain in the wells and high electric fields. One way to overcome these limitations is to diffract

29   the incident LWIR radiation from the vertical mode to an in-plane mode. Such diffraction is

30   preferably accomplished with a second-order diffraction grating incorporated between the top

31   mirror and the active device structure for the pixel element. In this configuration, the pitch of the

1    grating is preferably equal to the wavelength in the desired material. No blaze is required. The

2    LWIR energy may propagate equally in both directions. The grating acts in concert with the

3    vertical cavity. The resonant cavity causes only the desired wavelength of interest to resonate.

4    Every pass of the resonant LWIR energy through the grating diffracts the LWIR energy into the

5    in-plane mode (which is parallel to the surface and quantum wells of the pixel element). This

6    mode resonates back and forth in the active structure of the pixel element and is absorbed. In the

7    event that the quantum selection rule inhibits absorption, these modifications will enhance the

8    absorption of the pixel element.

9

10    In alternate embodiments, the thyristor-based pixel structure and corresponding method

11    of operation can be utilized to detect THz radiation. In this configuration, the resonant cavity is

12    not needed, and thus the top and bottom mirrors are omitted. Instead, one or more antenna

13    elements that are adapted to receive the desired THZ spectrum are operably coupled via

14    corresponding p-channel injector terminals to the p-type modulation doped quantum well

15    interface of the thyristor-based detector. Details of exemplary thyristor-based THz detectors is

16    set forth in International Application No. PCT/US03/13183, incorporated by reference above in

17    its entirety. Preferably, such thyristor-based THz detectors operate during the signal transfer

18    mode in each imaging cycle to empty the p-type modulation doped quantum well interface

19    (layers 1155c - 1158) of the thyristor-based THz detector of free holes, thereby forcing the p-

20    type modulation doped quantum well interface into a state of deep depletion. Preferably, this is

21    accomplished by biasing the cathode terminal electrode of the thyristor-based detector such that

22    conduction does not occur from the cathode terminal to the n-type quantum well interface of the

23    thyristor-based detector and applying a negative clock pulse to the p-channel injector terminal of

24    the thyristor-based detector such that the p-type modulation doped quantum well interface is

25    emptied of holes. Alternatively, this can be accomplished by holding the potential of the p-

26    channel injector terminal of the thyristor-based detector at a constant level and applying a

27    positive voltage pulse to the cathode terminal electrode of the thyristor-based detector such that

28    the p-type modulation doped quantum well interface is emptied of holes.

29

30    There have been described and illustrated herein several embodiments of thyristor-based

31    imaging arrays, thyristor-based CCD elements and thyristor-based detectors. While particular

1   embodiments of the invention have been described, it is not intended that the invention be

2   limited thereto, as it is intended that the invention be as broad in scope as the art will allow and .

3   that the specification be read likewise. Thus, while particular materials, fabrication processes,

4   circuit elements, and circuit architectures have been disclosed, it will be understood the others

5   can be used as well. In addition, while particular device structures have been disclosed, it will be

6   appreciated that others can be used as well. It will therefore be appreciated by those skilled in

7   the art that yet other modifications could be made to the provided invention without deviating

8   from its spirit and scope as claimed.